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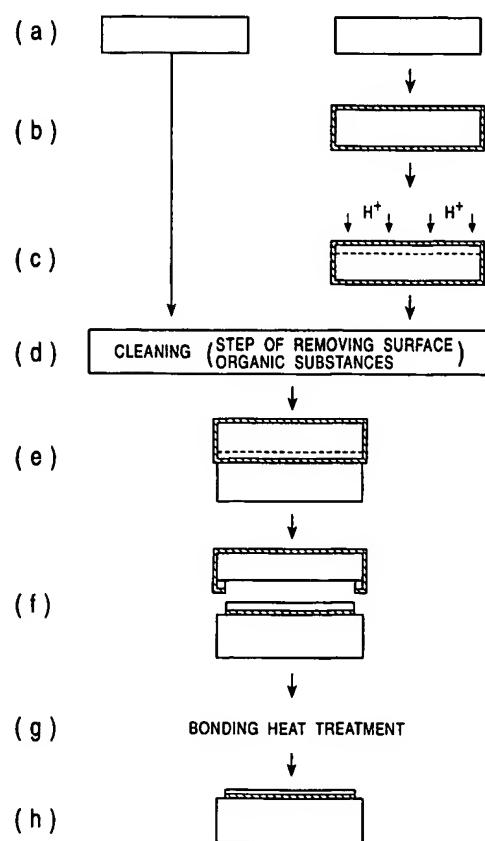
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### (54) Method for manufacturing bonded wafer and bonded wafer

(57) The object of the invention is to provide a bonded wafer in which an inferior bonding state of the bonded wafer attained by a hydrogen ion delamination method is reduced, no separation or no void is found at the connecting interface under a superior production characteristic and in a low cost. In a method for manufacturing a bonded wafer by a hydrogen ion delamination method, carbon concentration at a close contacted surface where both wafers are closely contacted from each other is  $3 \times 10^{14}$  atoms/cm<sup>2</sup> or less.

### FIGURE



**Description****2. Background of the Invention****Field of the Invention**

**[0001]** This invention relates to a method for reducing an inferior bonding at a joint surface in a so-called hydrogen ion delamination (separation) method (also called as a smart-cut method) in which joined SOI wafers at least one wafer being ion implanted are heat treated to cause separation to SOI wafers and delaminated wafers, thereafter the SOI wafers are heat treated to make bonding firmly.

**Description of the Related Art**

**[0002]** As a method of manufacturing an SOI (silicon on insulator) wafer under application of a bonding method, it has been well known in the related art to provide a technology for bonding two silicon wafers through a silicon oxide film, for example, a method for forming an oxide film on at least one wafer, closely contacting these wafers to each other without placing any foreign materials at the joint surface, thereafter heat treating them at a temperature of about 200 to 1200 °C to increase a bonding strength, as disclosed in the gazette of Japanese Patent Publication No. Hei 5-46086.

**[0003]** The bonded wafer of which bonding strength is increased through performing a heat treatment is enabled to be ground and polished after the treatment, so that the wafer applied to form an element is reduced in its thickness to a desired thickness under grinding and polishing operations and then it is possible to form the SOI layer forming an element.

**[0004]** The bonded SOI wafer made in this way has some advantages that it has a superior crystalline characteristic of the SOI layer and a high reliability in an buried oxide layer present just below the SOI layer. However, it was made thin through grinding and polishing, resulting in that it took much time for making a thin film, useless application of material was set and uniformity of film thickness of only about  $\pm 0.3 \mu\text{m}$  of a target film thickness was attained.

**[0005]** In turn, with a recent trend of high integration and high speed in operation of semiconductor devices, it is required to have further thin thickness of the SOI layer and a uniformity of film thickness and more practically, it is required to have a film thickness and its uniformity of about  $0.1 \pm 0.01 \mu\text{m}$ .

**[0006]** Realization that the thin film SOI wafers having such a film thickness as above and a uniform film thickness by a bonded wafer was impossible under a thickness reducing work through the related art grinding and polishing, so that as a new thin film forming technology, a method called as a hydrogen ion delamination (separation) method (also called as a smart cut method) disclosed in the gazette of Japanese Patent Laid-Open No.

Hei 5-211128 has been developed.

**[0007]** This hydrogen ion separation method is a technology in which an oxide film is formed on at least one of the two silicon wafers, either hydrogen ion or rare gas ion is implanted from the upper surface of one silicon wafer, a fine air bubble layer (enclosing layer) is formed in the silicon wafer, thereafter the ion implanted surface is closely contacted with the other wafer through the oxide film, a heat treatment (a separation heat treatment) is applied, one wafer is delaminated in a thin film state with the fine air bubble layer being applied as a separation surface (a delaminating surface), and further a heat treatment (a bonding heat treatment) is applied and they are forcedly bonded each other to make an SOI wafer.

**[0008]** This method has an advantage that the material can be used effectively due to the fact that the delaminating surface is a superior mirror surface and the SOI wafer having a quite high uniform characteristic of the SOI layer can be attained in a relative easy manner and further the delaminated one wafer can be utilized again.

**[0009]** In addition, this method also enables the silicon wafers to be directly bonded to each other without applying any oxide film, and this is used not only for a case in which the silicon wafers are bonded to each other, but also a case in which insulator wafers having different thermal expansion coefficients such as quartz, silicon carbide and alumina or the like after implanting ions into the silicon wafers.

**[0010]** In the case that the bonded wafers are made by such a hydrogen ion separation method, it is also possible to perform a heat treatment of high temperature also acting as a separation heat treatment and a bonding heat treatment at once as a post heat treatment after the two wafers are closely contacted to each other at a room temperature, although it is normally carried out that for a sake of convenience in use of the delaminated wafer after its heat treatment, the separation heat treatment is once carried out at a relative low temperature of about 500 °C, the delaminated wafer is recovered, only the SOI wafer is separately processed in a bonding heat treatment at a high temperature of about 1100°C, for example.

**[0011]** However, the present inventors found that the following two kinds of inferior bonding occurred frequently while the bonded wafer was being made in repetition by the hydrogen ion separation method.

1) Inferior bonding in which after performing the separation heat treatment, delaminated state does not occur at the ion implanted layer, but either an entire surface or its part is separated at the close contacted portions (joint surface);

2) Inferior bonding in which although a void (a partial unbonded portion) is not generated at all after performing a separation heat treatment, but void is generated after performing a bonding heat treatment.

[0012] In regard to the aforesaid two kinds of inferior bondings, the present inventors studied them honestly and found that these inferior bondings had a certain relation with a concentration of organic substances contained in the surfaces closely contacted to each other at a room temperature.

[0013] Further, describing it in detail, it is assumed that the phenomenon in which the organic substances may become a cause of void is generated in the case that the organic substances trapped at the joint surface are processed by a high temperature bonding heat treatment to become gasified, and if its gas pressure is superior to a bonding strength or rigidity of silicon, void is formed. Accordingly, in the case of the related art bonding method, since it is normally found that the bonded wafer is not made thin when a bonding heat treatment is carried out, if the wafer has a high rigidity and a relative small amount of organic substances is trapped at the joint surfaces, they may not become gasified and formed as void and they are diffused and diminished from the joint surface.

[0014] To the contrary, in the case of hydrogen ion delamination method, since a high temperature bonding heat treatment is carried out at the SOI layer after the separation heat treatment under a state of quite thin thickness of  $2 \mu\text{m}$  or less, the present inventors have found that rigidity of wafer is quite weak and even if such a small amount of organic substances trapped at the joint surface as one not producing any void under the related art bonding method is present, there occurs a phenomenon in which the void is generated only after the bonding heat treatment is carried out, as described in the above item 2).

[0015] In turn, the present inventors have found that occurrence of inferior bonding is dependent on a presence or a non-presence of a silicon oxide film or its thickness at the close contacted surfaces of the wafers. That is, if the bonding is performed through an oxide film, the gas generated under the presence of the organic substances is absorbed into the oxide film, so that the void is hardly formed. Then, it may be considered that this phenomenon shows a certain effect as a thickness of the oxide film is thicker.

### 3. Summary of the Invention

[0016] In view of the foregoing, the present invention has been attained in reference to a relation between an inferior bonding of the bonded wafers and a concentration of carbon atoms which can be an index for contamination of organic substances at the close contacted surface and it is a main object of the present invention to reduce an inferior bonding of the bonded wafers attained by the hydrogen ion delamination method and to provide the bonded wafers having no separation at the bonding interface or no void under a high productivity and a low cost.

[0017] In order to accomplish the aforesaid problem,

one aspect of the present invention is a method for manufacturing a bonded wafer by a hydrogen ion delamination method characterized in that carbon concentration at close contacted surfaces of both wafers is  $5 \times 10^{14}$  atoms/cm $^2$  or less.

[0018] As described above, if the carbon concentration at the close contacted surfaces where both wafers are closely contacted at a room temperature is  $5 \times 10^{14}$  atoms/cm $^2$  or less, no inferior bonding which no separation occurs at the ion implanted layer after performing the separation heat treatment, and either the entire surface or its part is separated at the close contacted surfaces is not produced.

[0019] In another aspect of the present invention, if carbon concentration at a joint surface after separation heat treatment is  $3 \times 10^{14}$  atoms/cm $^2$  or less, it is possible to prevent a void from being generated by its subsequent bonding heat treatment.

[0020] Preferably, a thickness of a silicon oxide film present at close contacted surfaces is  $0.1\mu\text{m}$  or more, thereby the occurrence of void caused by the bonding heat treatment can be positively prevented.

[0021] In further aspect of the present invention, if the surfaces of wafers to be bonded from each other are cleaned with ozone cleaning and/or sulfuric acid-hydrogen peroxide cleaning combined with at least one of SC-1 cleaning and SC-2 cleaning, thereafter the wafers are bonded to each other, carbon concentration at the close contacted and joint surfaces can be positively reduced to such a level as one where no void is generated.

[0022] Additionally, further aspect of the invention describes a bonded wafer characterized in that carbon concentration at the joint surfaces after a separation heat treatment is  $3 \times 10^{14}$  atoms/cm $^2$  or less. If such a wafer as one described above is applied, since generation of void can be prevented through high temperature bonding heat treatment, it is possible to manufacture the bonded wafers having high quality without any void in a high yield. In particular, in the case of bonded SOI wafer, it is preferable that a thickness of the silicon oxide film present at the joint surfaces is  $0.1\mu\text{m}$  or more.

[0023] As the wafer to be used for reducing an inferior bonding at the hydrogen ion separation method, it is preferable to apply a wafer having such a surface concentration as above in which carbon concentration at the close contacted surfaces of both wafers is  $3 \times 10^{14}$  atoms/cm $^2$  or less. In addition, in the case of manufacturing the bonded SOI wafer, it is preferable that a thickness of the silicon oxide film present at the close contacted surfaces is  $0.1\mu\text{m}$  or more.

[0024] As described above, the present invention can suppress inferior bondings in which after performing the separation heat treatment, delamination does not occur at the ion implanted layer, but either an entire surface or its part is separated at the close contacted portions, and although a void (partial unbonded portion) is not generated at all wafer after performing a separation heat treatment, but void is generated after performing a

bonding heat treatment, when the bonded wafer is manufactured by hydrogen ion delamination method. Accordingly, the bonded wafer having no separation state or void at the bonding interface can be provided in a superior productivity and under a low cost.

#### 4. Brief Description of the Drawings

**[0025]** Figure is a flow chart for indicating an example of manufacturing steps for the bonded SOI wafer in accordance with the present invention.

#### 5. Description of the Preferred Embodiments

**[0026]** Referring now to Figure, one preferred embodiment of the present invention will be described. However, the present invention is not limited to this preferred embodiment. In this case, Figure is a flow chart for indicating one example of manufacturing steps of the bonded SOI wafer of the present invention.

**[0027]** At the step (a), two silicon wafers 1, 2 are prepared, wherein both wafers are single-crystal silicon wafers in which at least surfaces to be bonded are polished in mirror surface. In this Figure, 1 denotes a base wafer and 2 denotes a bond wafer.

**[0028]** The step (b) is a step for forming an oxide film 3 at the bond wafer 2 becoming the SOI layer. Since the oxide film 3 becomes a buried oxide layer of the SOI wafer, its thickness is set in response to its application, although about 0.1 to 2.0 $\mu$ m is normally applied. In addition, it is also preferable that an oxide film is not formed at the bond wafer 2, but the oxide film is formed at the base wafer 1 becoming the supporting wafer for the SOI layer and also both of them may be formed with oxide films.

**[0029]** Then, at the step (c), at least one of hydrogen ion or rare gas ion, hydrogen ion in this case is implanted from above the upper surface of one surface of the bond wafer 2 (a surface bonded to the base wafer 1) and then a fine air bubble layer (enclosing layer) 4 in parallel with the surface at a mean penetration depth of ion is formed, wherein it is preferable that a temperature of wafer during implantation operation is 25 to 450 °C and in particular, 200 °C or less is preferable.

**[0030]** At the step (d), this is a cleaning step in which surface impurities are removed before the base wafer 1 and the bond wafer 2 are closely contacted at a room temperature. This related art cleaning step was carried out such that mixed solution of ammonium hydroxide and hydrogen peroxide called as SC-1 cleaning, or mixed solution of hydrogen chloride and hydrogen peroxide called as SC-2 cleaning are applied independently or under a combination of several steps. However, in the present invention, in addition to the SC-1 cleaning or SC-2 cleaning, a combined method of a well-known ozone cleaning (pure water containing ozone) or sulfuric acid-hydrogen peroxide cleaning (mixed solution of concentrated sulfuric acid and hydrogen peroxide water) is

carried out in order to perform an effective removal of the organic substances at the surface. With such an arrangement as above, the organic substances at the surfaces of the base wafer 1 and the bond wafer 2 can be removed effectively, so that it is possible that a concentration of carbon at the close contacted surfaces closely contacted to each other at a room temperature is positively set to  $5 \times 10^{14}$  atoms/cm<sup>2</sup> or less.

**[0031]** In addition, since a concentration of carbon at the close contacted surfaces is determined in response to cleaning conditions such as a temperature, composition and cleaning time of the cleaning liquid at the step (d), if a relation between the cleaning condition and the concentration of carbon at the close contacted surfaces is checked in advance, a cleaning condition which is most suitable for the target concentration of carbon can be set.

**[0032]** As a measuring method, there may be provided TD-GC-MS (Thermal Desorption Gas Chromatography Mass Spectroscopy) method or SIMS (Secondary Ion Mass Spectroscopy) under application of a thin film SOI to be described later.

**[0033]** Then, at the step (e), this is a step in which both wafers after their cleaning are superposed to each other and closely contacted to each other, wherein the surfaces of the two wafers are contacted to each other in a clean atmosphere at a normal temperature, thereby the wafers are closely joined to each other without using any adhesive agent or the like.

**[0034]** At the step (f), this is a separation heat treatment in which a delaminated wafer 5 and the SOI wafer 6 (SOI layer 7 + buried oxide layer 3 + base wafer 1) are separated while being delaminated with the enclosing layer 4 being applied as an interface, wherein, for example, if a heat treatment is applied at a temperature of about 500 °C or more in inert gas atmosphere, the delaminated wafer 5 and the SOI wafer 6 are separated by a rearrangement of crystals and cohesion aggregation of air bubbles and concurrently the close contacted surfaces at a room temperature are rigidly bonded to a certain degree. At this step, an analysis with SIMS (Secondary Ion Mass Spectroscopy) is carried out from the SOI surface of the SOI wafer 6 toward its depth direction, resulting in that a specified amount of concentration

of carbon at the close contacted surface at a room temperature can be specified in its quantity. In addition, if a reclaiming processing in which the oxide film 3 at the surface is removed and the delaminated surface is polished is carried out, the delaminated wafer 5 can be utilized again.

**[0035]** In order to use the SOI wafer 6 during the device manufacturing step, a bonding strength under a separation heat treatment at the step (f) is insufficient, so that the heat treatment at high temperature is applied as a bonding heat treatment at the step (g) so as to cause the bonding strength to be sufficiently high. This heat treatment can be carried out in an atmosphere of inert gas, for example, at a temperature of about 1000

to 1200 °C for about 30 minutes to 5 hours. In addition, if a rapid heating and rapid cooling device such as a lamp heating device is applied, a sufficient bonding strength can be attained at a temperature of about 1000 to 1350 °C for a short period of 1 to 300 seconds.

[0036] Then, at the step (h), this is a step in which a damaged layer and a surface roughness present at the delaminated surface (separated surface) acting as the surface of the SOI layer 7 are removed. As this step, a polishing process called as a touch-polish having a quite less amount of stock removal or a heat treatment can be carried out in a reducing atmosphere containing hydrogen after the touch polishing operation. However, even if only the heat treatment is carried out in the reducing atmosphere containing hydrogen without performing the touch-polishing, the damaged layer and the surface roughness can be similarly removed and further it may act as the bonding heat treatment at the step (g), resulting in that a more efficient step can be assured.

[Preferred Embodiment]

[Example 1]

[0037] At first, two single-crystal silicon wafers 2 having a diameter of 150 mm, a thickness of 625 µm, a conductive p-type, and a resistivity of 10 to 20 Ω·cm with its one surface being polished in mirror surface were prepared, one of the wafers was formed as a bond wafer and an oxide film having a thickness of 0.1 µm was formed at the surface by a thermal oxidation.

[0038] Then, H + ions were implanted at the mirror surface side of the bond wafer through an oxide film under a condition of an implanting energy of 40 keV and an implanting dose  $8 \times 10^{14}$  atoms/cm<sup>2</sup>, thereafter sulfuric acid-hydrogen peroxide cleaning (96% concentrated sulfuric acid: 30% H<sub>2</sub>O<sub>2</sub> = 6 kg: 100 cc, a liquid temperature of 110 °C) was carried out for 5 minutes, rinsed with pure water, thereafter SC-1 cleaning (29% NH<sub>4</sub>OH aqueous solution: 30% H<sub>2</sub>O<sub>2</sub>, pure water = 1 : 1 : 8, a liquid temperature of 80 °C) was carried out for 4 minutes, and further SC-1, SC-2 (36% HCl aqueous solution: 30% H<sub>2</sub>O<sub>2</sub>: pure water = 1 : 1 : 6, a liquid temperature of 80 °C) and SC-1 were carried out in sequence for every 4 minutes.

[0039] In turn, SC-1, SC-2 and SC-1 cleanings were carried out in sequence for every 4 minutes without performing a sulfuric acid-hydrogen peroxide cleaning, both wafers were dried, thereafter they were closely contacted to each other at a room temperature and further as a separation heat treatment, the heat treatment at 500 °C was carried out for 30 minutes in nitrogen gas atmosphere.

[0040] As a result, the SOI wafer having a thickness of the SOI layer of about 0.25 µm and the delaminated wafer were made as shown in step (f) of Figure. Visual inspection of the SOI wafer after its separation showed that the void was not observed at all. If the SOI layer is

kept at its thin-film state, the portion where the void is present is seen as a protruded shape, so that the void can be observed without using any special device.

[0041] Then, the bonding heat treatment was carried out for this SOI wafer in nitrogen gas atmosphere at 1100 °C for 2 hours. The SOI wafer after its bonding heat treatment was observed visually and no void was observed at all.

[0042] In addition, up to the separation heat treatment was carried out under the quite same condition as that of the aforesaid operation, the SOI wafer separately manufactured was diced, SIMS measurements were carried out for three portions (a portion near its center, a portion near 35 mm from its center and a portion near 65 mm from its center), carbon concentration at the close contacted surface at a room temperature was calculated to find out a value of  $3 \times 10^{14}$  atoms/cm<sup>2</sup> or less.

[Example 2]

[0043] The bond wafer in which the wafer of the same kind as that of the preferred embodiment 1 was not formed with an oxide film, but ion implanted under the same condition was manufactured and kept in a desiccator containing dibutylbenzoquinone therein for 1 hour.

[0044] After this period, the cleaning with sulfuric acid-hydrogen peroxide was not carried out, but only the SC-1, SC-2 and SC-1 cleanings were carried out under the same condition as that of the preferred embodiment 1 together with the base wafer and after drying them, both wafers were closely contacted to each other at a room temperature, the same separation heat treatment and bonding heat treatment as those of the preferred embodiment 1 were carried out in sequence. As a result, several voids with a diameter of about 2 to 10 mm were generated at the SOI wafer after the separation heat treatment and their numbers at the SOI wafer were increased after the bonding heat treatment was carried out. However, a phenomenon in which the entire surface of the SOI wafer is separated after performing the separation heat treatment was not occurred.

[0045] In addition, up to the separation heat treatment was carried out under the quite same condition as that of the aforesaid operation, the bonded wafer separately manufactured was diced, SIMS measurements were carried out for three portions (a portion near its center, a portion near 35 mm from its center and a portion near 65 mm from its center), carbon concentration at the close contacted surface at a room temperature was calculated to find out a value of  $5 \times 10^{14}$  atoms/cm<sup>2</sup> or less.

[Example 3]

[0046] Except the fact that an oxide film with a thickness of 0.1 µm was formed at the bond wafer, a plurality of SOI wafers were manufactured in which operations up to the bonding heat treatment were carried out in sequence under the same condition as that of the pre-

ferred embodiment 2. As a result, no voids were observed at all at any kinds of SOI wafers after performing the separation heat treatment, although there occurred cases in which several voids were generated after performing the bonding heat treatment and the other cases in which voids were not generated at all.

[Comparative Example 1]

[0047] A bond wafer in which an oxide film was not formed in the same kind of wafer as that shown in the preferred embodiment 1 and ion implantation was carried out under the same condition was manufactured, and kept in a desiccator containing dibutylbenzoquinone therein for 6 hours.

[0048] After this period, the cleanings SC-1, SC-2 and SC-1 were carried out in sequence under the same condition as that of the preferred embodiment 1 only for the base wafer and after drying them, both wafers were closely contacted to each other at a room temperature, the same separation heat treatment as that of the preferred embodiment 1 was carried out.

[0049] As a result, entire surfaces of both wafers after separation heat treatment were separated at an interface closely contacted at a room temperature and no delamination of the wafer at the ion implanted layer was found.

[0050] In addition, after a silicon layer of about  $0.3\text{ }\mu\text{m}$  was deposited at  $600\text{ }^{\circ}\text{C}$  in a reduced pressure by a vapor phase growth apparatus after the surface of the bond wafer had been processed up to the step keeping it in a container under the quite same condition as the foregoing. Then SIMS measurement was carried out in the same manner as those of the preferred embodiments 1 and 2, carbon concentration at the surface of the bond wafer was calculated to find out a value of  $5 \times 10^{14}\text{ atoms/cm}^2$  or higher.

[Comparative Example 2]

[0051] Except the fact that an oxide film with a thickness of  $0.1\mu\text{m}$  was formed at the bond wafer, operations up to the separation heat treatment were carried out under the same condition as that of the comparative example 1. As a result, a part of the interface closely contacted at a room temperature was separated.

[0052] Further, the present invention is not limited to the aforesaid preferred embodiments. The aforesaid preferred embodiments are illustrative, and have a substantial same configuration as that of the technical concept described in the claims of the present invention and so any type of embodiments showing the similar actions and effects are included in the technical scope of the present invention.

[0053] For example, although the manufacturing step for the SOI wafer of the present invention is illustrated in Figure for the case in which the oxide film is formed only at the bond wafer, it may also be applicable that the

oxide film is formed only at the base wafer or oxide films may be formed at both wafers. In addition, the present invention may be adapted for the case in which it is bonded as base wafer to insulator wafers having different thermal expansion coefficients such as polycrystalline silicon or quartz, silicon carbide, alumina or the like.

[0054] Having described specific examples of the invention with reference to the accompanying drawings, it will be appreciated that the present invention is not limited to those precise embodiments, and that various changes and modifications can be effected therein by one of ordinary skill in the art without departing from the scope of the invention as defined by the appended claims.

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Claims

1. A method for manufacturing a bonded wafer by a hydrogen ion delamination method, wherein carbon concentration at close contacted surfaces of both wafers is  $5 \times 10^{14}\text{ atoms/cm}^2$  or less.
2. A method for manufacturing a bonded wafer by a hydrogen ion delamination method, wherein carbon concentration at a joint surface after separation heat treatment is  $3 \times 10^{14}\text{ atoms/cm}^2$  or less.
3. A method for manufacturing a bonded wafer according to claim 1 and 2, wherein thickness of a silicon oxide film present at close contacted surfaces is  $0.1\mu\text{m}$  or more.
4. A method for manufacturing a bonded wafer by a hydrogen ion delamination method, wherein surfaces of wafers to be bonded to each other are cleaned with ozone cleaning and/or sulfuric acid-hydrogen peroxide cleaning combined with at least one of SC-1 cleaning and SC-2 cleaning, thereafter the wafers are bonded to each other.
5. A bonded wafer manufactured by a hydrogen ion delamination method, wherein a concentration of carbon at the joint surface after a separation heat treatment is  $3 \times 10^{14}\text{ atoms/cm}^2$  or less.
6. A bonded wafer according to claim 5, wherein a thickness of a silicon oxide film present at a joint surface is  $0.1\mu\text{m}$  or more.
7. A wafer applied in a hydrogen ion delamination method, wherein carbon concentration at a close contacted surface where two wafers are closely contacted to each other is  $5 \times 10^{14}\text{ atoms/cm}^2$  or less.
8. A wafer applied in a hydrogen ion delamination method according to claim 7, wherein a thickness

of a silicon oxide film present at close contacted surfaces is 0.1µm or more.

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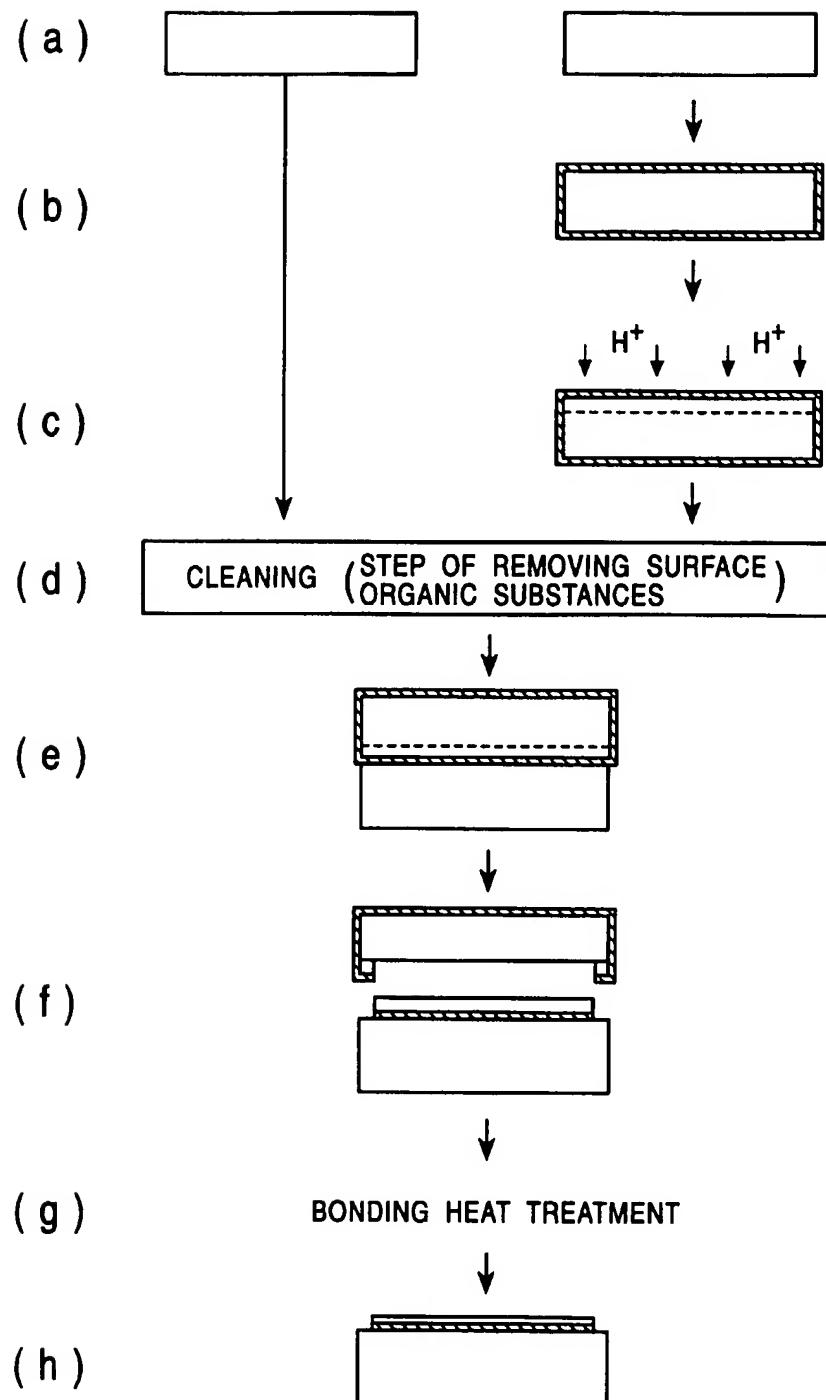
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# FIGURE





European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 99 30 5525

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	H01L21/20 H01L21/762 H01L21/306
X	MALEVILLE C ET AL: "Wafer bonding and H-implantation mechanisms involved in the Smart -cut(R) technology" MATERIALS SCIENCE AND ENGINEERING B, vol. 46, no. 1-3, 1 April 1997 (1997-04-01), page 14-19 XP004085270 ISSN: 0921-5107 * page 14, paragraph 2 - page 15, left-hand column; figure 1 * * page 16 - page 18, left-hand column; figures 4-7 *	1,2,5,7	H01L21/20 H01L21/762 H01L21/306
Y	---	3,4,6,8	
Y	EP 0 476 897 A (SHINETSU HANDOTAI KK) 25 March 1992 (1992-03-25) * page 4, line 24 - line 27 * * page 4, line 45 - line 54 * * page 5, line 8 - page 6, line 8 * * page 6, line 21 - line 22; table 1 * * page 7, line 4 - line 31; figures 2A-2F *	3,6,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
A	---	1,2,4,5, 7	H01L
Y	US 5 773 355 A (INOUE SHUNSUKE ET AL) 30 June 1998 (1998-06-30) * column 5, line 10 - line 22; figure 1 * * column 5, line 31 - column 5, line 13; figures 3-5 * * column 10, line 55 - column 12, line 14; figures 23-27 *	4	
A	---	1-3,5-8	
		-/--	
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
BERLIN		27 October 1999	Klopfenstein, P
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			
T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons S : member of the same patent family, corresponding document			



European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number

EP 99 30 5525

DOCUMENTS CONSIDERED TO BE RELEVANT									
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (InLCl.7)						
A	<p>FUJIMO S ET AL: "SILICON WAFER DIRECT BONDING THROUGH THE AMORPHOUS LAYER" JAPANESE JOURNAL OF APPLIED PHYSICS, vol. 34, no. 10B, PART 02, 15 October 1995 (1995-10-15), pages L1322-L1324, XP000702224 ISSN: 0021-4922 * page L1322, paragraph 2; figure 1 *</p> <p>-----</p>	1,4,5,7							
			TECHNICAL FIELDS SEARCHED (InLCl.7)						
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>BERLIN</td> <td>27 October 1999</td> <td>Klopfenstein, P</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	BERLIN	27 October 1999	Klopfenstein, P
Place of search	Date of completion of the search	Examiner							
BERLIN	27 October 1999	Klopfenstein, P							
<p>CATEGORY OF CITED DOCUMENTS</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; vertical-align: top;">           X : particularly relevant if taken alone            Y : particularly relevant if combined with another document of the same category            A : technological background            O : non-written disclosure            P : intermediate document         </td> <td style="width: 50%; vertical-align: top;">           T : theory or principle underlying the invention            E : earlier patent document, but published on, or after the filing date            D : document cited in the application            L : document cited for other reasons            .....            8 : member of the same patent family, corresponding document         </td> </tr> </table>				X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document	T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ..... 8 : member of the same patent family, corresponding document				
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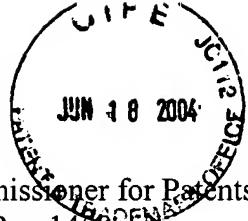
ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.

EP 99 30 5525

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

27-10-1999

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
EP 0476897	A	25-03-1992	JP	1997176 C	08-12-1995
			JP	4119626 A	21-04-1992
			JP	7019739 B	06-03-1995
			US	5232870 A	03-08-1993
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US 5773355	A	30-06-1998	JP	7283380 A	27-10-1995
			EP	0676796 A	11-10-1995
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The following items listed below are being filed herewith with the USPTO on June 18, 2004.

Express Mail No. <b>EV 346 811 198 US</b>			
Attorney Docket No.	Appln. Serial No./ Patent No.	Items - Documents filed on <u>June 18, 2004</u>	Patent Fees- Acct. #50-1814
4717-10500	10/808,288	Response to Notice to File Missing Parts of NonProvisional Application; Copy of Notice; Executed Inventors Declaration (2 pgs.); Copy of Application ; Executed Power of Attorney to Prosecute Application Before The USPTO with Statement Under 37 CFR 3.73(b) and copy of Assignment; Supplemental Information Disclosure Statement, PTO 1449, 2 refs.	\$130 <i>840</i>

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